WHAT IS CLAIMED IS:

1. Apparatus having an interface port for simultaneously transmitting and receiving input and output signals, comprising:

a first circuit for generating an output signal;

a second circuit having a first terminal and a second terminal, the first terminal coupled to the first circuit, the second terminal coupled to the interface port, a signal level at the first terminal representing a first combination of the input and output signals, and a signal level at the second terminal representing a second combination of the input and output signals; and

a third circuit coupled to the first and second terminals of the second circuit for determining the input signal based on the signal levels at the first and second terminals.

2. The apparatus of Claim 1, wherein the second circuit comprises a resistor, the first terminal comprises a first end of the resistor, and the second terminal comprises a second end of the resistor.

3. The apparatus of Claim 1, wherein the third circuit processes the first and second combinations of the input and output signal levels to generate a signal that corresponds to the input signal.

4. The apparatus of Claim 1, wherein the third circuit multiplies the first combination of the input and output signal levels by a first constant to generate a first number and multiplies the second combination of the input and output signal levels by a second constant to generate a second number, the difference between the second and the first numbers corresponding to the input signal.

5. The apparatus of Claim 4, wherein the interface port is coupled to a transmission line having an impedance of Z, the second circuit has a resistance of Ra, and the ratio between the first constant and the second constant is approximately equal to Z / (Z + Ra).

6. The apparatus of Claim 4, wherein the interface port is coupled to a transmission line having an impedance of Z via a resistance of Rc, the interface port being coupled to electric ground via a resistance of Rb, the second circuit having a resistance of Ra, and the ratio between the first constant and the second constant being approximately equal to Rb*(Z+Rc)/(Rb*(Z+Rc)+Ra*(Rb+Rc+Z)).

7. An integrated circuit comprising:

a first circuit for providing a variable output signal;

an internal impedance having a first terminal and a second terminal, the first terminal electrically connected to the first circuit;

an interface port electrically connected to the second terminal of the internal impedance, a signal level at the interface port corresponding to a combination of the variable output signal and an input signal from an external circuit; and

a second circuit for processing the signal levels at the first and second terminals at the internal impedance to generate a signal that corresponds to the input signal from the external circuit.

8. The apparatus of Claim 7, wherein the second circuit multiplies a signal level at the first terminal of the internal impedance by a first constant to generate a first number and multiplies a signal level at the second terminal of the internal impedance by a second constant to generate a second number, the difference between the second and the first numbers corresponding to the input signal.

9. The apparatus of Claim 8, wherein the interface port is coupled to a transmission line having an impedance of Z, the second circuit has a resistance of Ra, and the ratio between

the first constant and the second constant is approximately equal to Z / (Z + Ra).

10. The apparatus of Claim 8, wherein the interface port is coupled to a transmission line having an impedance of Z via a resistor having a resistance of Rc, the interface port being coupled to electric ground via a resistance of Rb, the second circuit having a resistance of Ra, and the ratio between the first constant and the second constant being approximately equal to Rb (Z + Rc) / (Rb (Z + Rc) + Ra (Rb + Rc + Z)).

11. A system comprising:

a transmission line having a first end and a second end;

a first driver for generating a first output signal;

a first bridge having a first terminal for coupling to the first driver and a second terminal for coupling to the first end of the transmission line;

a second driver for generating a second output signal;

a second bridge having a first terminal for coupling to the second driver and a second terminal for coupling to the second end of the transmission line;

a first arithmetic unit for processing signal levels of the first and second terminals of the first bridge to generate a first computed signal that corresponds to the second output signal; and

a second arithmetic unit for processing signal levels of the first and second terminals of the second bridge to generate a second computed signal that corresponds to the first output signal.

12. The system of Claim 11, wherein the first bridge comprises a first resistor, the first terminal of the first bridge comprises a first end of the first resistor, the second terminal of the first bridge comprises a second end of the first resistor, the second bridge comprises a second resistor, the first terminal of the second bridge comprises a first end of the second resistor, and the second terminal of the second bridge comprises a second end of the second resistor.

13. The system of Claim 11, wherein the first arithmetic unit multiplies a signal level at the first terminal of the first bridge by a first constant to generate a first number and multiplies a signal level at the second terminal of the first bridge by a second constant to generate a second number, the difference between the second and the first numbers corresponding to the input signal.

14. The system of Claim 13, wherein the transmission line has an impedance of Z, the first bridge has a resistance of Ra, and the ratio between the first constant and the second constant is approximately equal to Z / (Z + Ra).

15. The apparatus of Claim 13, wherein the transmission line has an impedance of Z, the first bridge has a resistance of Ra, the second terminal of the first bridge is coupled to electric ground via a resistance of Rb, the second terminal of the first bridge is coupled to the transmission line via a resistance of Rc, and the ratio between the first constant and the second constant is approximately equal to Rb*(Z+Rc)/(Rb*(Z+Rc)+Ra*(Rb+Rc+Z)).

16. A memory chip comprising:

an interface pin for simultaneously reading in write data to the memory chip and sending out read data from the memory chip;

a driver for generating the read data;

an internal impedance having a first and a second terminals, the first terminal being electrically coupled to the driver and the second terminal being electrically coupled to the interface pin; and

an arithmetic unit for processing signal levels of the first and second terminals of the internal impedance and for generating a signal corresponding to the write data.

17. The memory chip of Claim 16, wherein the arithmetic unit multiplies a signal level at the first terminal by a first constant to generate a first number and multiplies a signal

level at the second terminal by a second constant to generate a second number, the difference between the second and the first numbers corresponding to the write data.

18. The memory chip of Claim 16, wherein the interface pin is coupled to a transmission line having an impedance of Z, the internal impedance has an impedance of Ra, and the ratio between the first constant and the second constant is approximately equal to Z / (Z + Ra).

19. The memory chip of Claim 16, wherein the interface pin is coupled to a transmission line having an impedance of Z via a resistance of Rc, the interface pin being coupled to electric ground via a resistance of Rb, the internal impedance having an impedance of Ra, and the ratio between the first constant and the second constant being approximately equal to Rb*(Z+Rc)/(Rb*(Z+Rc)+Ra*(Rb+Rc+Z)).

20. A system comprising:

a data bus having a first end and a second end;

a processor for generating write data, the processor having a first interface port and a first arithmetic unit, the first interface port being coupled to the first end of the data bus; and

a memory for generating read data, the memory having a second interface port and second arithmetic unit, the second

interface port being electrically coupled to the second end of the data bus;

wherein the write data is sent from the processor to the memory via the data bus at the same time that the read data is sent from the memory to the processor via the data bus, the first arithmetic unit processing combinations of the write and read data to generate a first computed signal corresponding to the read data, and the second arithmetic unit processing combinations of the read and write data to generate a second computed signal corresponding to the write signal.

21. The system of Claim 20, wherein the processor further comprises a first driver and a first bridge, the first driver generating the write data, the first bridge having a first terminal coupled to the first driver and a second terminal coupled to the first end of the data bus, the first arithmetic unit processing the signal levels at the first and second terminals of the first bridge to generate the first computed signal.

22. The system of Claim 21, wherein the first arithmetic unit multiplies the signal level at the first terminal of the first bridge by a first constant to generate a first number and multiplies the signal level at the second terminal of the first bridge by a second constant to generate a second number,

the difference between the second and the first numbers corresponding to the read signal.

23. The system of Claim 20, wherein the memory further comprises a second driver and a second bridge, the second driver generating the read signal, the second bridge having a first terminal coupled to the second driver and a second terminal coupled to the second end of the data bus, the second arithmetic unit processing the signal levels at the first and second terminals of the second bridge to generate the second computed signal.

24. The system of Claim 23, wherein the second arithmetic unit multiplies the signal level at the first terminal of the second bridge by a third constant to generate a third number and multiplies the signal level at the second terminal of the second bridge by a fourth constant to generate a fourth number, the difference between the fourth and the third numbers corresponding to the write signal.

25. A system comprising:

a data bus having a first end and a second end;

a first device comprising:

a first driver for generating a first output signal,

a first bridge having a first terminal for coupling to the first driver and a second terminal for coupling to the first end of the data bus, and

a first arithmetic unit; and

a second device comprising:

a second driver for generating a second output signal,

a second bridge having a first terminal for coupling to the second driver and a second terminal for coupling to the second end of the data bus, and

a second arithmetic unit;

wherein the first arithmetic unit processes signal levels of the first and second terminals of the first bridge to generate a first computed signal that corresponds to the second output signal, and the second arithmetic unit processes signal levels of the first and second terminals of the second bridge to generate a second computed signal that corresponds to the first output signal.

26. The system of Claim 25, wherein the first device is a computer.

27. The system of Claim 26, wherein the second device is a disk drive.

28. The system of Claim 26, wherein the second device is an input/output device.